IN THE SPECIFICATION:

Please amend paragraph **[0001]** as follows:

[0001] This application is a continuation of application Serial No. 09/211,089, filed December 14, 1998, now U.S. Patent No. 6,342,789 B1, issued January 29, 2002, which is a divisional of application Serial No. 08/643,518, filed May 6, 1996, now U.S. Patent 5,905,382, issued May 18, 1999, which is a continuation of application Serial No. 07/981,956, filed November 24, 1992, now U.S. Patent 5,539,324, issued July 23, 1996, which is a continuation-in-part of application Serial No. 07/575,470, filed August 29, 1990, abandoned, and shares common subject matter with application Serial No. 07/709,858, filed June 4, 1991, ~~abandoned~~ abandoned, and application Serial No. 07/788,065, now U.S. Patent No. 5,440,240, issued August 8, 1995.

Please amend paragraph **[0003]** as follows:

[0003] State of the Art: Semiconductor devices are subjected to a series of test procedures in order to confirm functionality and yield, and to ~~assure~~ ensure quality and reliability. This testing procedure conventionally includes "probe testing," in which each individual ~~dice,~~ die, while still on a wafer, ~~are~~ is initially tested to determine functionality and speed. Probe cards are used to electrically test dice at that level. The electrical connection interfaces with only a single die at a time in a wafer before the ~~dice are~~ die is singulated from the wafer.

Please amend paragraph **[0004]** as follows:

[0004] If the wafer has a yield of functional dice ~~which~~ that indicates that quality of the functional dice is likely to be good, each individual die is traditionally assembled in a package to form a semiconductor device. Conventionally, the packaging includes a lead frame and a plastic or ceramic housing.

Please amend paragraph **[0005]** as follows:

[0005] The packaged devices are then subjected to another series of tests, which include burn-in and discrete testing. Discrete testing permits the devices to be tested for speed and for errors ~~which~~ that may occur after assembly and after burn-in. Burn-in accelerates failure mechanisms by electrically exercising the devices (devices under test or DUT) at elevated temperatures and elevated dynamic biasing schemes. This induces infant mortality failure mechanisms and ~~elicit~~ elicits potential failures ~~which~~ that would not otherwise be apparent at nominal test conditions.

Please amend paragraph **[0006]** as follows:

[0006] Variations on these procedures permit devices assembled onto circuit arrangements, such as memory boards, to be burned-in, along with the memory board in order to ~~assure~~ ensure reliability of the circuit board and the circuit board assembly and manufacturing process, as populated with devices. This closed assembly testing assumes that the devices are discretely packaged in order that it can then be performed more readily.

Please amend paragraph **[0008]** as follows:

[0008] It is proposed that devices be packaged without conventional lead frames. This creates two problems for conventional test methods. Firstly, discrete testing is more difficult because the conventional lead frame package is not used. Furthermore, multiple devices may be assembled into a single package, thereby reducing the performance of the package to ~~that~~ those of the die with the lowest performance. This is because the ability to presort the individual dice is limited to that obtained through probe testing. Secondly, the packaging may have other limitations of package assembly defect mechanisms ~~which~~ that are aggravated by burn-in stress conditions so that the packaging becomes a limitation for burn-in testing.

Please amend paragraph **[0013]** as follows:

[0013] This technique allows all elements of the burn-in/test fixture to be 100% reusable, while permitting testing of each individual ~~dice~~ die in a manner similar to that accomplished with discrete packaged semiconductor devices.

Please amend paragraph **[0016]** as follows:

[0016] Characterization, such as speed grading, is even more variable than yield. While a packaged DRAM is purchased by the consumer based on the parts' speed grade, speed grading of probe wafers is almost a matter of conjecture. ~~That~~ This means that it is happenchance as to whether the assembly house purchases a wafer of mostly "-10" parts (100 ns) or mostly "-6" parts (60 ns).

Please amend paragraph **[0017]** as follows:

[0017] Recent developments in fabrication technology have resulted in such speed characterizations being more uniform on any given wafer. This has made it possible to provide wafers in which a majority of good dice have speed grades ~~which~~ that do not greatly exceed an average for the wafer. Such uniformity, along with an ability to achieve fuse repairs and patches, ~~have~~ has made wafer scale integration of arrays and cluster packaging practical.

Please amend paragraph **[0018]** as follows:

[0018] Other developments include an ability to track individual dice on wafers, starting at probe. Traditionally, probe identifies bad dice (for example, an ink spot). The assembly process is continued only for dice ~~which~~ that do not have the ink spots. By computer tracking, the ink spot becomes superfluous, as a map of good and bad dice are stored and transferred to subsequent assembly steps.

Please amend paragraph **[0021]** as follows:

[0021] According to the present invention, burn-in and testing are accomplished on an uncut wafer by mounting the wafer to a reusable burn-in/test fixture. The test fixture has contact

tips thereon in order that electrical contact may be established for each individual ~~dice~~ die on the wafer. The fixture consists of two halves, one of which is a wafer cavity plate for receiving the wafer as the devices under test (DUT), and the other half establishes electrical contact with the wafer and with a burn-in oven.

Please amend paragraph **[0023]** as follows:

[0023] The contact tips are electrical contact locations at which the electrical contact is established by the fixture. These may be flat contact areas ~~which~~ that mate with bumps on the wafer, raised electrical bumps or resilient fingers. The wafer itself may use either flat bond pads or raised bump contacts.

Please amend paragraph **[0028]** as follows:

[0028] This technique allows most or all elements of the burn-in/test fixture to be 100% reusable, while permitting testing of each individual ~~dice~~ die while on the wafer in a manner similar to that accomplished with discrete packaged semiconductor devices.

Please amend paragraph **[0036]** as follows:

[0036] In the preferred embodiment, a probe plate is fabricated on a substrate 63 (FIG. 4) and has conductive patterns therein. The conductive patterns terminate in conductive bumps (for example) or pads. It is also possible to form the substrate 63 so that it is thin enough to be at least flexible. By way of example, such a substrate 63 may be formed from silicon or ceramic, which has been made thin enough that it is able to be flexed substantially more than the wafer 30. Circuit traces on the substrate 63 communicate with individual contacts on the edge connectors 23′. This permits the edge connectors 23′ to be used to connect the contact pads on the dice with external electrical equipment (not shown). While the edge connectors 23′ are shown as being generally aligned with the individual ~~dies~~ dice on the wafer, it is possible to have the circuit traces extend to any convenient location on the substrate 63.

Please amend paragraph **[0037]** as follows:

[0037] Alternatively, by making the substrate thin enough or by using a flexible material, it is possible to use a flexible substrate ~~which~~ that is, by its nature, more likely to conform to the wafer 30. This flexible substrate can be combined with a rigid support (not shown) to make the substrate semi-rigid.

Please amend paragraph **[0041]** as follows:

[0041] The support plate 12 includes a floating platform 41 ~~which~~ that is supported by a biasing mechanism 43. The wafer 30 is held in place in the wafer receiving cavity 17 by the floating platform 41. In the embodiment shown, the biasing mechanism 43 is an elastomeric polymer, although coil springs or the like can be used. The purpose of the biasing mechanism 43 is to bias the floating platform 41 upwards so that when the wafer 30 is inserted into the wafer receiving cavity 17 and the fixture is assembled, the wafer will be in contact with the contact tips 31. The biasing force of the biasing mechanism 43 and the travel of the floating platform 41 must be uniform enough and provide enough travel that when the wafer receiving cavity 17 receives a wafer, and the support plate 12 is mounted to the wafer cavity plate 11, the contact tips 31 will each contact the die pads. As a result of the uniformity of travel and biasing, the mating of the wafer cavity plate 11 and the support plate 12 need only accommodate the need to provide an even biasing of the wafer 30 against the contact tips 31 to a degree sufficient for each contact tip 31 to contact its respective die pad. This means that lateral alignment, as established by the dowels 27 and dowel-receiving cavities 28, is more critical than the precise closeness of the support plate 12 to the wafer cavity plate 11.

Please amend paragraph **[0043]** as follows:

[0043] It is possible to use address circuitry in order to reduce the number of external connectors ~~which~~ that would be otherwise necessary in order to perform complete testing of the circuits on the wafer 30. In this manner, an entire wafer can be tested with a small number of connections. An example of an appropriate address circuit would be an address and self test circuit arrangement used on a computer memory board.